Data Acquisition System for the Sensirion Humidity and Temperature Sensors

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This note gives an overview of the data acquisition (DAQ) system that has been developed for the Sensirion humidity and temperature, SHT85, sensors [1], which are planned for use in Hall B's second RICH detector.

The DAQ system [2] developed for the FPGA-based SHT85 sensors comprises two main code sections—FPGA Command Engine (FCE) [3] and the System Scan Engine (SSE), which has an autoscan and a manual operation mode. The overview of the DAQ system is shown in Fig. 1.

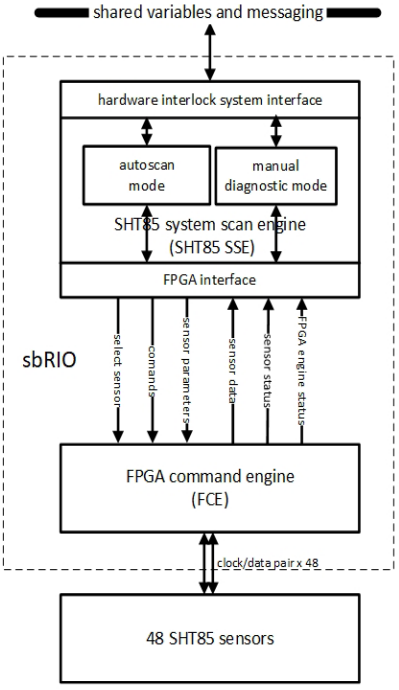

FIG. 1. DAQ system block diagram.

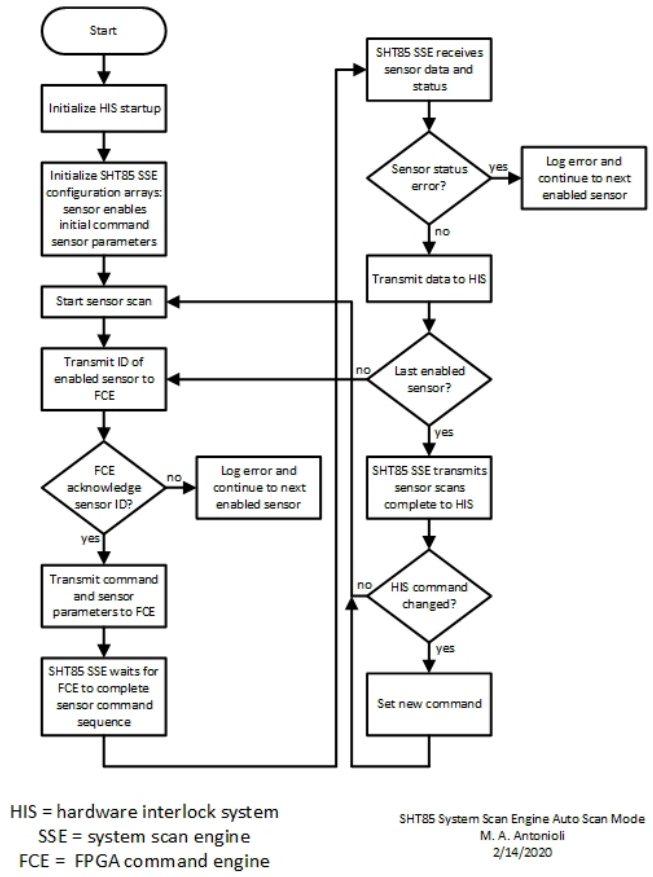

FIG. 2. Flowchart for the autoscan operation mode.

The flowchart for the autoscan mode is shown in Fig. 2. At cycle start, upon initialization, the Hardware Interlock System transmits the array of enabled sensors, their operation parameters (e.g. timing delays), and the selected command to SSE via LabVIEW-shared variable arrays.

SSE communicates to FCE the ID of the first enabled sensor from the array of enabled sensors. Once SSE confirms the sensor ID was received by FCE, the command to be executed and the operation parameters are transmitted by SSE to FCE.

Based on this information, FCE generates I^2C serial commands [4], communicates with the enabled sensor, and transmits data received from the sensor to SSE.

The command sequence ends when sensor data and sensor status are received by the Hardware Interlock System interface.

The scan cycle continues with the next enabled sensor. The scan cycle ends when the last enabled sensor completes the issued command, at which point, prior to the start of the next cycle, the Hardware Interlock System interface can instruct SSE to continue executing the same command again or issue a new command.

Error checking is performed throughout the cycle. Should an error occur, the event is logged and email is sent to system experts. SSE will not transmit data to the Hardware Interlock System interface if the data is associated with a cycle fault.

The manual mode, which can be entered at the reset of the Hardware Interlock System or in between autoscan mode cycles, is used by system experts for diagnostics, for resetting of sensors, and for a detailed DAQ performance analysis.

Since the sensors are not accessible once the RICH detector has been assembled, having dedicated wiring to each of the 48 SHT85 sensors ensures that the failure of a sensor will not affect the performance of the others. Therefore, from the sbRIO-9627 CompactRIO Single-Board Controller [5], clock and data pair signals are wired individually to the 48 sensors.

In conclusion, DAQ for the SHT85 sensors has been developed, tested, and debugged. The DAQ supports all functions needed to program, read, and transmit data from sensors to the Hardware Interlock System.

[1] P. Bonneau, et al., *Proposed Integrated Temperature and Humidity Digital Sensor for the RICH Detector*, DSG Note 2019-12, 2019.

[2] P. Bonneau, et al., *Development of Data Acquisition to Read out Sensirion SHT85 Temperature and Humidity Sensors for the RICH Detector*, DSG Note 2019-31, 2019.

[3] P. Bonneau, et al., *FPGA Command Engine Development for the RICH Hardware Interlock System*, DSG Note 2020-02, 2020.

[4] P. Bonneau, et al., *Proposed Controller for the Readout of the Temperature and Humidity Digital Sensors Sensirion SHT85 Envisioned for the RICH Detector*, DSG Note 2019-27, 2019.

[5] P. Bonneau, et al., *Developing a Readout System for the Sensirion SHT85 Sensors*, DSG Note 2019-28, 2019.